ABSTRACT

An object of the present invention is to provide an interleaver and a deinterleaver, which are small-sized and power saving. An address converter ACON has three counters CNT1, CNT2 and CNT3 in associated with a first rank through a third rank and the outputs DO11, DO12 and DO13 of respective counters CNT1, CNT2 and CNT3 are inputted in lookup tables LUT1, LUT2 and LUT3. In the counter CNT3, a clock CK1 with a predetermined cycle is inputted and the numeric values of "0" through "3" are repeatedly outputted. In the counter CNT2, a carry out CO3 to be outputted in synchronization with the output of the counter CNT3, i.e., "0" is inputted as a clock CK2. Further, the counter CNT2 outputs the numeric values of "0" through "4" repeatedly. In the counter CNT1, a carry out CO2 to be outputted in synchronization with the output of the counter CNT2, i.e., "0" is inputted as a clock CK3. Further, the counter CNT1 outputs the numeric values of "0" through "15" repeatedly.